Tuesday May 21st

15h30 to 17h30 Lecture Subramanian S. Iyer

(Samueli School of Engineering, University of California , Los Angeles USA) Makalu Room

Packaging- When all else fails! Or Why I became a packaging Engineer

Co-Organized with IEEE Advancing Technology for Humanity | IEEE Electronics Packaging Society | FRANCE SECTION

Wednesday May 22nd

8h45 **Welcome to MiNaPAD**

9h00 Opening by Alexandre Val (Auditorium)

9h30 ***Keynote 1: Subramanian S. Iyer***
"A Moore's law for packaging" (Auditorium)

10h15 **Exhibition Opening (Exhibition Hall)**

	Session A : MEMS & LED	Session B : Process Optimization
10h45	CMOS Image Sensor Packaging Technology (T.E. Kang, UTAC Group)	Copper Wire Robustness for High Volume Production (F. Quercia, ST Microelectronics)
11h10	Curved Full-Frame CMOS Sensor: Impact on Electro-Optical Performances (B. Chambion, CEA-LETI)	Packaging for the Automotive Industry (L. Chemisky, YOLE Développement)
11h35	A New Method for a Failure Characterization of a Flip-Chip Assembly of pixelated LED Light Source Package (S. Beddar, Versailles Saint-Quentin University)	Sawing Capability Study for Front-Side Chipping Reduction (M. Tumiati, ST Microelectronics)

12h00–13h15 Lunch (Exhibition Hall– Exhibition)

13h15 ***Keynote 2: Jacques Fournier (CEA-LETI): Secure Packaging for Addressing Hardware Security Challenges (Auditorium)***

Session C : Interposer 2.5D/TSV/3D

14h30 New Copper and Cobalt wet metallization enabling multiple Integrations for FEOL and BEOL (C. Doussot, AVENI)

14h55 Layout Design of I/O Libraries for Wirebond & Flip-Chip Package options (K. Chanumolu, ARM)

15h20 Metrology for High Density Wafer Level Fan-Out & TSV based stacking (D.Alliata, UNITYSC)

15h45 Advanced Packaging Material Developments for 3D Stacking and System-In –Package (R. De Witt, Henkel Electronics Materials

16h00-16h40 Exhibition/coffee break sponsored by ASE GROUP

	Session D : Dicing/Picking 1	Session E : PCB1-Embedded
16h40	Plasma Dicing: A Device-Enabling Technology for advanced Packaging and 3D Integration (P.Bezard, PLASMA-THERM)	EHDICOS “Embedded Technologies” with standards Components (F. Lechleiter, CIMULEC)
17h05	A more than Moore Enabling Wafer Dicing Technology (J. van Borkulo, ASMPT)	EDDEMA: Embedded Die Design Environment and Methodology for Automotive Applications (N. Marier, VALEO)
17h30	Development of Back Gridding/Mask 2 in 1 Tape for Plasma Dicing Process (T. Uchimaya, FURUKAWA ELECTRIC)	Advanced PCB Technology for Integrated Flexible Electronics (J. Verhegge, ACB)

18h00-18h30 **Exhibition**

19h30 **Social Event - Restaurant** “Les Jardins de Sainte Cécile”

Thursday May 23rd

8h30 ***Keynote 3: Jean-Marc Yannou (ASE): Car Electrification: a revolution also for the semiconductor packaging marketing (Auditorium)***

	Session F : Characterization/Reliability	Session G : Advanced Process
9h30	Mechanical Behavior of SAC305 Lead free Alloy (J. Vieilledent, THALES GLOBAL SERVICES)	Innovative Implementation of additive Manufacturing for Advanced Microelectronics Packaging (A. Roshangias, CTR)
9h55	Thermomechanical Behavior Characterization new Development for high Resolution multi-scale Analyses (D. Ecoiffier, INSIDIX)	Increased Integration Density of optoelectronic Modules by Through-Silicon Laser Soldering adapted for Wafer Level Packaging (K. Worth, FICONTEC)
10h20	A comprehensive Methodology for Design for Package Miniaturization (R. Duca, ST Microelectronics)	Moisture uptake of PECVD dielectrics at ambient and accelerated Test Conditions (H. Fremont, Laboratory IMS)

10h45-11h10 Exhibition/coffee break sponsored by

	Session H : SiP	Session I : Joining/Advanced Process
11h10	Miniaturized Medical Devices (P. von Meiss, VALTRONIC)	Statistical Study of SAC Solder joints in QFN and BGA assemblies (H. Fremont, Laboratory IMS)
11h35	Evolution of RF SiP and challenges ahead (C. Zinck, ASE)	Key Advances In Void Reduction and Warpage Mitigation in the Reflow Process (J. Balackyi, HELLER Industries)

12h00– 13h00 Lunch & Exhibition (Exhibition hall)

13h00 ***Keynote 4: Olivier Coulon (DECISION): Electronics in Europe (Auditorium)***

	Session J : PCB2-Power	Session K : Dicing/Picking 2
13h35	To be completed (IRT)	Adhesion strength of Epoxy Molding Compound to metals in a semiconductor package (F. Viviani, St Microelectronics)
14h00	Double Side Interconnection for vertical power components based on Macro and Nano structured Copper Interfaces and printed Circuit Board Technologies (B.Djuric, MITSUBISHI Electric)	Packaging of a MOEMS LIDAR Sub Assembly for distance Metering on a 3D housing (J. Abdilla, BESI AT)
14h25	To be completed (ELVIA)	Laser-lift-off (LLO) and CONDOx for Wafer ultra-thinning process for 3D stacked Devices, TSV, eWLB and WLCSP and DICING WITHOUT Adhesives for MEMS and optical devices (G. Klug, DISCO)

15h00-15h20 Exhibition / Coffee Break

15h20 ***Keynote 5: YOLE/SYSTEM PLUS To be completed (Auditorium)***

16h15 Best Paper Awards

16h30 End of MiNaPAD2019